Abstract

A method for mapping an electronic digital circuit to a Look Up table (LUT) based Programmable Logic Deviceoperates by selecting an unmapped or partially mapped LUT, and identifying a group of circuit elements for mapping on the selected LUT based on the available capacity of the selected LUT and the mapping constraints. The identified circuit elements are mapped onto the selected LUT. The identification of circuit elements and mapping is carried out while taking into consideration the Cascade Logic associated with the selected LUT. The process continues until all circuit elements have been mapped. The group of circuit elements is mapped to the cascade logic prior to mapping on the LUTs. Conversely, the cascade logic is incorporated only after all circuit elements have initially been mapped onto LUTs or some elements remain unmapped after all LUTs have been utilized. The mapping constraints include timing, placement, and size constraints.